

FIG. 3

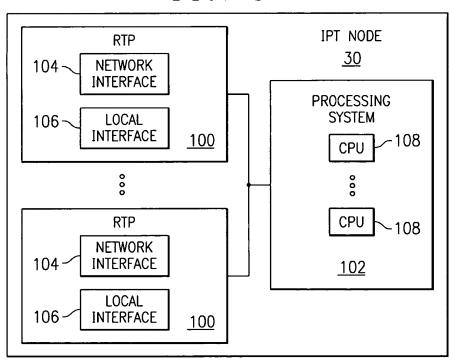




FIG. 4

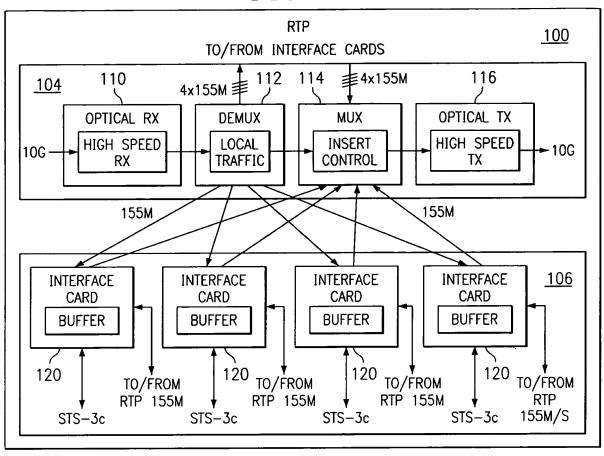


FIG. 7

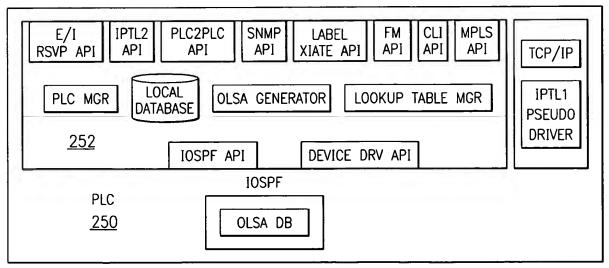




FIG. 5A

FIG. 58 2

BB MGR 102 CONTROL COMPONENT SUBSYSTEMS 168 PLATFORM COMPONENT IPTL2 MASTER (TR1) 170 MODEL (TR1) IPTL2 ARCHITECTURE IPTL2 0SPF 166 -156 MGR BB COMPONENT SUBSYSTEMS 150/ CONTROL IPTL2 MANAGEMENT SLAVE (TR1, TR2, TR3) PLATFORM COMPONENT IPTL1 MASTER IPTL2 SLAVE ME MODELS 152 IPTL1 ARCHITECTURE IPTL1 ME MODEL IPTL1 OSPF 154~ 146~

09

PROCESSING SYSTEM

CPU 1

4

CPU 2

SNMP AGENT/IPTL2MIB (TR1)

162~

SNMP AGENT/IPTL1 MIB

142~

CMIB

148

CMIB

144~

7164

IPTL2 MASTER ME



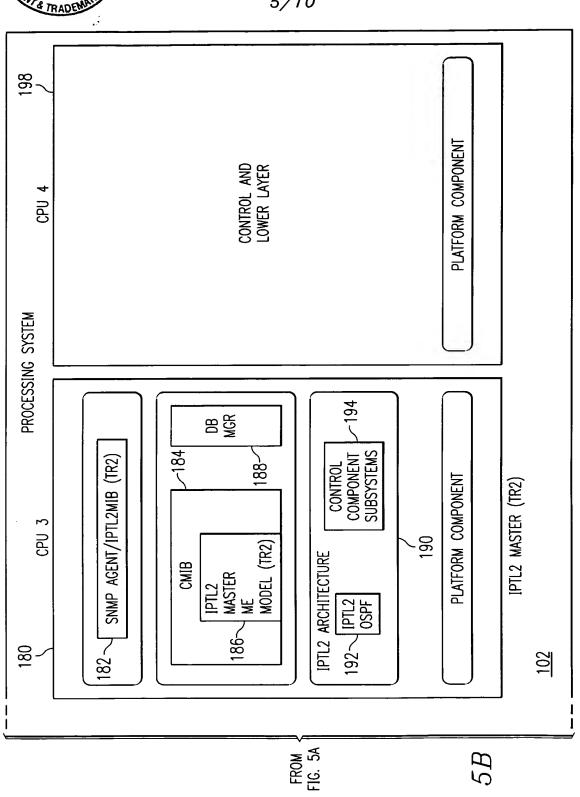
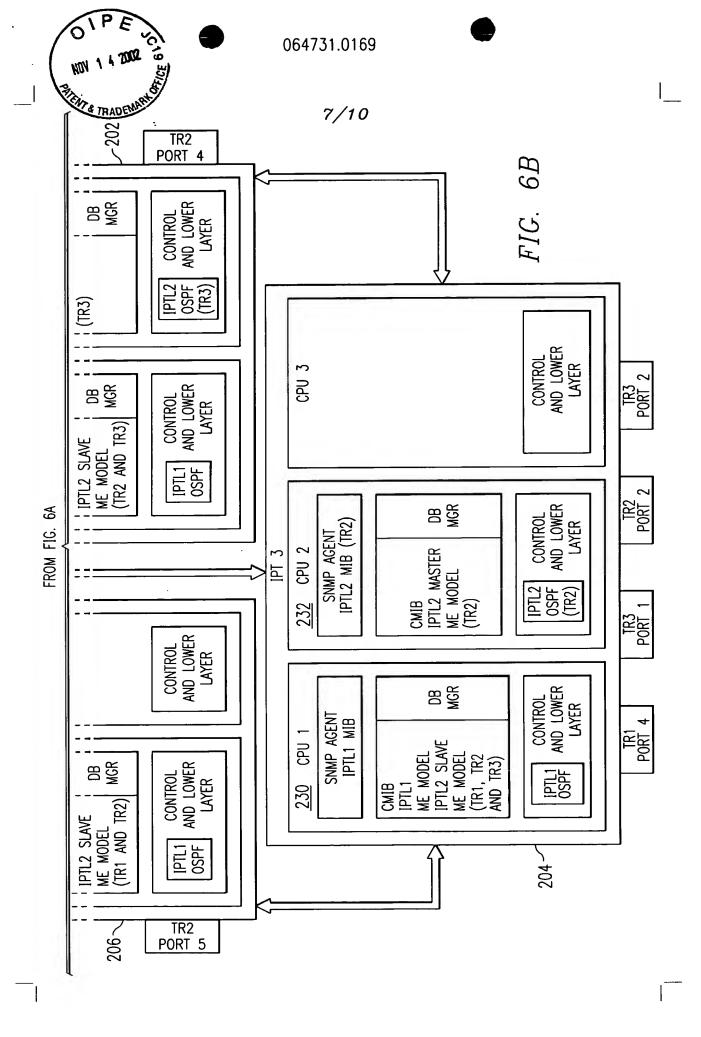
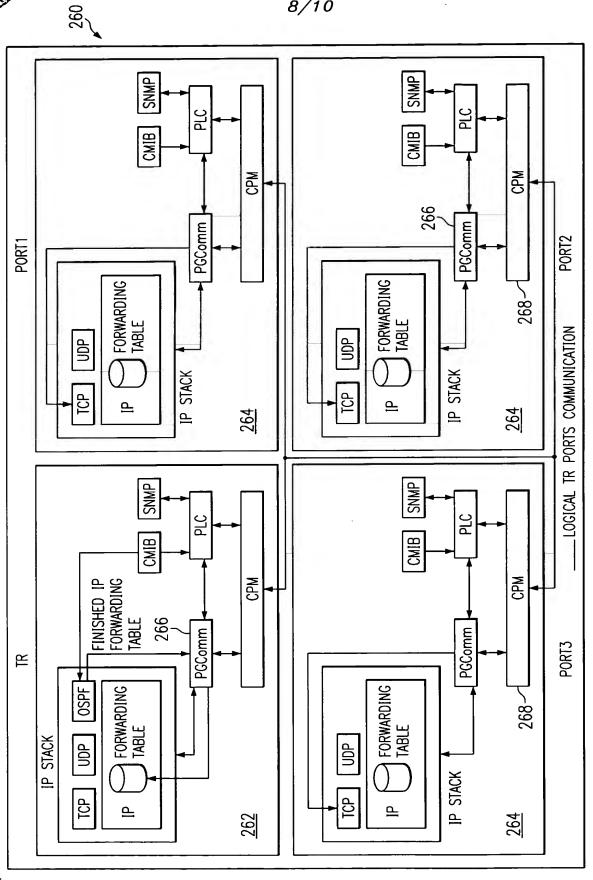


FIG. 5B

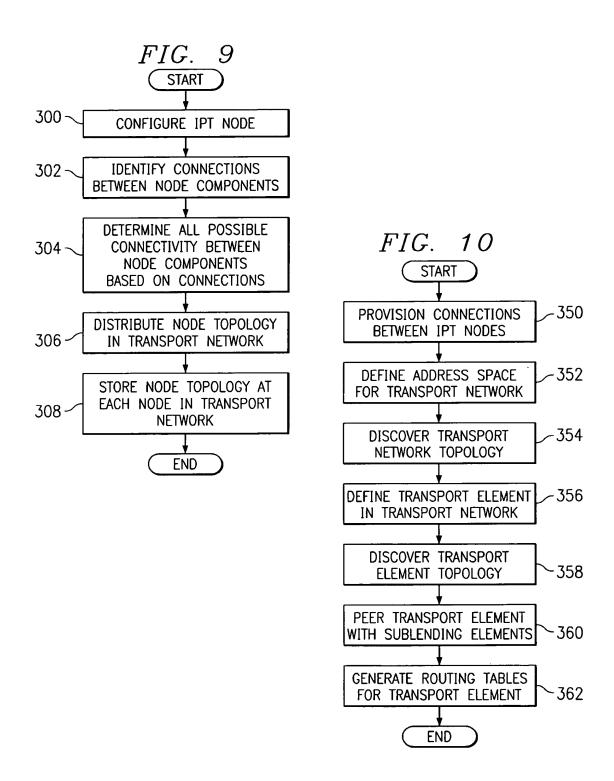






 ∞





END